Join the World of Image Processing

SILICONSOFTWARE

FULL x1 / FULL x4

microEnable IV



Ideal solution for advanced image acquisition and image processing with a flexible and scalable product concept

microEnable IV-FULL CHARACTERISTICS

- Performance solution for image acquisition and image processing
- Ultimative PCI Express performance
- Highly flexible and scalable product concept
- Numerous add-on boards for highest connectability

microEnable IV-FULL FEATURES

- All CameraLink conform cameras with Base, Medium and Full Configuration supported
- Single and Quad Lane PCI Express interfaces
- 256 and 512 MB DDR-RAM on-board
- FPGA and on-board memory for preprocessing
- Highly reliable image acquisition
- Intuitive interface for an easy frame grabber and camera configuration
- Graphical and intuitive interface to program FPGA vision processors by VisualApplets®
- VisualApplets® compatible interface
- Additional extension boards for special features
- Included software package: microDisplay, Software Development Kit (SDK), Diagnosis tool



VisualApplets compatible

PCI Express v.1.2 compliant

CameraLink v.1.2 compliant

microEnable IV-FULL family is a PCIe based product line. The boards offer an exceptional image acquisition and processing performance. microEnable IV uses the experienced frame grabber technology with its high reliability, stability and robustness. Both board types cope even with advanced requirements of applications by the additional FPGA capabilities for customized adaptations with VisualApplets®.

Standard Features:

- Support of all gray CameraLink input formats (Single/Dual Tap, 8/10/12/14/16 bit/pixel)
- Max. image display size 16,383 x 65,536 pixels, max. pixel clock 85MHz, frequency up to 20,000 frames/s and settable exposure
- Transfer rate of up to 760 MB/s on PCIe quad lane or 200 MB/s on PCIe single lane systems
- · On-board pixel reshuffling with support of various sensor readout strategies
- Knee Look-Up Table for piecewise linear conversion from 16 bit/pixel to 16 bit/pixel
- Internal 12 or 16bit processing
- · Basic image processing, e. g. brightness, contrast and gamma-correction.
- · White balancing
- · Hardware generated image number
- Regions of Interest support
- 8bit or 16bit output per color component (Gray8/Gray16 or RGB24/RGB48)
- Image selector
- · Latency of a single line
- Highly customizable trigger system
- Support of RS232 clser interface
- · Camera detection abilities
- DigI/O and CC signals

Special Features:

- On-board Bayer Pattern interpolation (bi-linear, 8 bit input, 9 bit precision, correct edge handling)
- On-board Bayer filter demosaicing (high quality, 12bit precision, correct edge handling)
- On-board 1D (line scan cameras) or 2D (area scan cameras) Shading correction, which adjusts offset and gain for each pixel separately to rectify inherent distortions from the sensor and/or illumination
- On-board Shading Correction at full bandwidth
- On-board Fixed Pattern Noise Correction
- Shaft Encoder A/B support (revolving direction detection and compensation)
- · Software trigger control
- Additional support for non-standard serial RGB formats, which enable RGB with higher bit/pixel through a CameraLink Base configuration (RGB assembled from Single Tap 8, 10, 12, 14, 16, and Dual Tap 8, 10, 12 at up to 85 MHz)

Bayer Filter: A Bayer filter is a color filtering array for arranging RGB colors on a monochromatic grid. The Bilinear Demosaicing Algorithm for Bayer Filters performs the color reconstruction according to a 3*3 reconstruction matrix. The calculations are performed with up to 12bit/ pixel. The High Quality (HQ) Demosaicing Algorithm for Bayer Filters performs the color reconstruction according to a 7*5 reconstruction matrix with special edge treatment. The calculations are performed with up to 12bit/ pixel accuracy.

Any information without obligation. Technical specifications and scope of delivery are liability-free and valid until revocation. Mistakes are excepted.



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Technical Specifications

Camera Interface:

- CameraLink interface with Base, Medium and Full Configuration
- All CameraLink conform cameras supported
- Pixel clock 85MHz

PC Interface:

• PCI host interface PCIe x1 or x4

Performance Data:

- Xilinx Spartan 3 XC3S 1600E or 4000 FPGA
- 256MB or 512MB on-board DDR-RAM memory

Available Product Types:

- microEnable IV FULL x1
- microEnable IV FULL x4

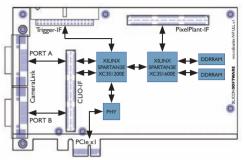
Available Add-on Boards:

- TTL and opto trigger boards
 - 8 inputs and 8 outputs
 - Both ports identical
 - Usable with included software package (microDisplay, SDK)
 - Usable with VisualApplets

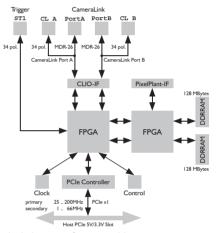
- CameraLink Input / Output (CLIO)
 - · Fixed plug
- Distribute camera data for up to 256 frame grabber
- Complex calculations: Images will be divided per image number or part of an image
- Different calculation methods on original image
- PixelPlant
 - PX100
 - Xilinx Spartan 3 XC3S 1600E FPGA
 - 256MB DDR-RAM
 - 1GB/s read + write
 - PX200
 - Xilinx Spartan 3 XC3S 4000 FPGA
 - 512MB DDR-RAM
 - 1GB/s read + write

Available Software Products:

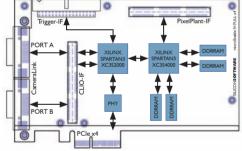
- VisualApplets®
- microDisplay
- microDiagnosis
- microEnable SDK



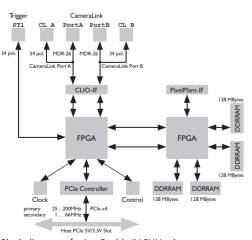
Scematic layout of microEnable IV-FULL x1



Block diagram of microEnable IV-FULL x1



Scematic layout of microEnable IV-FULL x4



Block diagram of microEnable IV-FULL x4

Supported Features Sorted by Hardware Applets for

microEnable IV-FULL x2 microEnable IV-FULL x4

CameraLink
Camera Type

Color Processing

Image Enhancement

Image Correction

Acquisition Modes

Performances

Image Formats
Transfer Rates

es re Applets for LL x1 LL x4	Single Area Bayer HQ	Single Area Gray Shading 16	Dual Area Bayer 12	Dual Area Gray 16	Dual Area RGB 48	Dual Line Gray 16	Dual Line RGB 30	MEDIUM Area Gray 16	MEDIUM Area RGB 36	MEDIUM Line Gray 16	MEDIUM Line RGB 36	FULL Area Gray 8	FULL Line Gray 8
BASE Configuration													
MEDIUM Configuration													
FULL Configuration													
Area Scan / Line Scan	Α	Α	Α	Α	Α	L	L	Α	Α	L	L	Α	L
GrayScale / RGB / Bayer	BAY	G	BAY	G	RGB	G	RGB	G	RGB	G	RGB	G	G
1- / 2-Camera Operation	1	1	2	2	2	2	2	1	1	1	1	1	1
White Balancing													
Bayer Filter Feature													
Bayer Bilinear Algorithm													
Bayer High Quality Algorithm													
Knee-LUT Table													
Image Processing													
Sensor Correction													
Shading Correction 1D													
Shading Correction 2D													
Image Selector													
Area Trigger													
Line Trigger													
Shaft Encoding													
Max. width (in k pixels)	4	8	4	16	16	16	4	8	2	16	16	2	16
Max. height (in k lines)	64	4	64	64	64	64	64	64	64	64	64	64	64
Image frequency (in k fps)	10	10	10	20	20	10	10	10	10	10	10	10	10
Gray8 or RGB24													
Gray16 or RGB 48													
FULL x1 (in MB/s)	200	200	200	200	200	200	200	200	200	200	200	200	200
FULL x4 (in MB/s)	680	230	750	380	600	380	600	700	600	700	600	640	640

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